CLAIMS

What is claimed is:

1. A process for fabricating a leadless plastic chip carrier, comprising:

selectively etching a leadframe strip to reduce a thickness of said strip at a portion thereof;

selectively masking said surface of said leadframe strip using a mask to provide exposed areas of said surface at said portion and contact pad areas on leadframe said strip;

depositing at least one layer of metal on said exposed areas to define a die attach pad on the portion of said leadframe strip with reduced thickness and to define contact pads on said surface of said strip;

mounting at least one semiconductor die to said die attach pad;

wire bonding said at least one semiconductor die to ones of said contact pads;

covering said at least one semiconductor die, said wire bonds, and said contact pads with an overmold material;

etching said leadframe strip to thereby remove said leadframe strip; and

singulating said leadless plastic chip carrier from said leadframe strip.

2. The process according to claim 1, wherein said selectively etching comprises:

depositing a photo-imageable etch resist on at least one surface of said leadframe strip;

imaging and developing said etch resist to expose said surface at said portion; and

etching said leadframe strip to thereby reduce the thickness of said strip at said portion.

3. The process according to claim 1, additionally comprising removing said mask prior to covering said at least one semiconductor die.

4. The process according to claim 1, wherein said depositing at least one layer of metal

comprises depositing a plurality of layers of metal on said exposed areas to define said die attach pad and said contact pads.

5. The process according to claim 1, additionally comprising:

masking said die attach pad after depositing said at least one layer;

depositing at least one further layer of metal on said at least one layer of metal at said contact pads thereby further defining said contact pads; and

stripping the mask from said die attach pad and said mask from said surface of said leadframe strip, prior to mounting said at least one semiconductor die.

6. The process according to claim 5, wherein depositing at least one metal comprises depositing layers of gold, nickel and copper, or silver and copper, or palladium, nickel and copper.

7. The process according to claim 6, wherein depositing at least one further layer of metal comprises depositing layers of nickel and gold, or silver, or nickel and palladium.

8. The process according to claim 1, wherein mounting at least one semiconductor die comprises mounting a plurality of semiconductor dice in a stack and wire bonding comprises fixing wire bonds between each of said semiconductor dice and ones of said contact pads.

9. A process for fabricating a leadless plastic chip carrier, comprising:

selectively etching a leadframe strip to reduce a thickness of said strip at a portion thereof;

selectively masking said surface of said leadframe strip using a mask to provide exposed areas of said surface at said portion and contact pad areas on said strip;

depositing a plurality of layers of metal on exposed areas to define a die attach pad on the portion of said strip with reduced thickness and to define contact pads on said surface of said strip;

masking said die attach pad after depositing said at least one layer;

depositing at least one further layer of metal on said at least one layer of metal at said contact pads thereby further defining said contact pads;

stripping the mask from said die attach pad and said mask from said surface of

said leadframe strip;

mounting at least one semiconductor die to said die attach pad;

wire bonding said at least one semiconductor die to ones of said contact pads;

covering said at least one semiconductor die, said wire bonds, and said contact pads with an overmold material;

etching said leadframe strip to thereby remove said leadframe strip; and

singulating said leadless plastic chip carrier from said leadframe strip.

10. The process according to claim 9, wherein mounting at least one semiconductor die comprises mounting a plurality of semiconductor dice in a stack and wire bonding comprises fixing wire bonds between each of said semiconductor dice and ones of said contact pads.

11. The process according to claim 9, wherein depositing said plurality of layers of metal comprises depositing layers of gold, nickel and copper, or silver and copper, or palladium, nickel and copper.

12. The process according to claim 9, wherein depositing at least one further layer of metal comprises depositing layers of nickel and gold, or silver, or nickel and palladium.

13. The process according to claim 1, further comprising fixing a plurality of solder ball contacts on said contact pads after said etching said leadframe strip to thereby remove said leadframe strip.

14. The process according to claim 9, further comprising fixing a plurality of solder ball contacts on said contact pads after said etching said leadframe strip to thereby remove said leadframe strip.

15. A leadless plastic chip carrier comprising:

a die attach pad;

at least one semiconductor die mounted on said die attach pad;

a plurality of contact pads circumscribing said die attach pad;

a plurality of wire bonds connecting said at least one semiconductor die and various ones of said contact pads; and

an overmold covering said semiconductor die and said contact pads,

wherein said die attach pad is offset from said contact pads such that said die attach pad protrudes from said molding compound.

16. The leadless plastic chip carrier according to claim 15, further comprising a plurality of solder balls disposed on said contact pads.

17. The leadless plastic chip carrier according to claim 15, further comprising a ground ring on a periphery of said die attach pad, said plurality of wire bonds further comprising wire bonds connecting said semiconductor die and said ground ring.

18. The leadless plastic chip carrier according to claim 15, further comprising a power ring intermediate said contact pads and said die attach pad, said plurality of wire bonds further comprising wire bonds connecting said semiconductor die and said power ring.

19. The leadless plastic chip carrier according to claim 15, wherein said at least one semiconductor die comprises a plurality of semiconductor dice stacked on top of each other and said plurality of wire bonds comprises wire bonds connecting ones of said plurality of semiconductor dice and ones of said contact pads.

20. The leadless plastic chip carrier according to claim 19, wherein adjacent ones of said semiconductor dice are separated by a layer of epoxy.

21. The leadless plastic chip carrier according to claim 19, further comprising a plurality of solder balls disposed on said contact pads.

22. The leadless plastic chip carrier according to claim 15, wherein said die attach pad comprises a plurality of layers of metal.

23. The leadless plastic chip carrier according to claim 15, wherein said contact pads comprise a plurality of layers of metal.

24. The leadless plastic chip carrier according to claim 22, wherein said plurality of layers of metal includes layers of gold, nickel and copper, or silver and copper, or palladium, nickel and copper.

25. The leadless plastic chip carrier according to claim 23, wherein said plurality of layers of metal includes layers of nickel and gold, or silver, or nickel and palladium.